

CAMAC Equipment

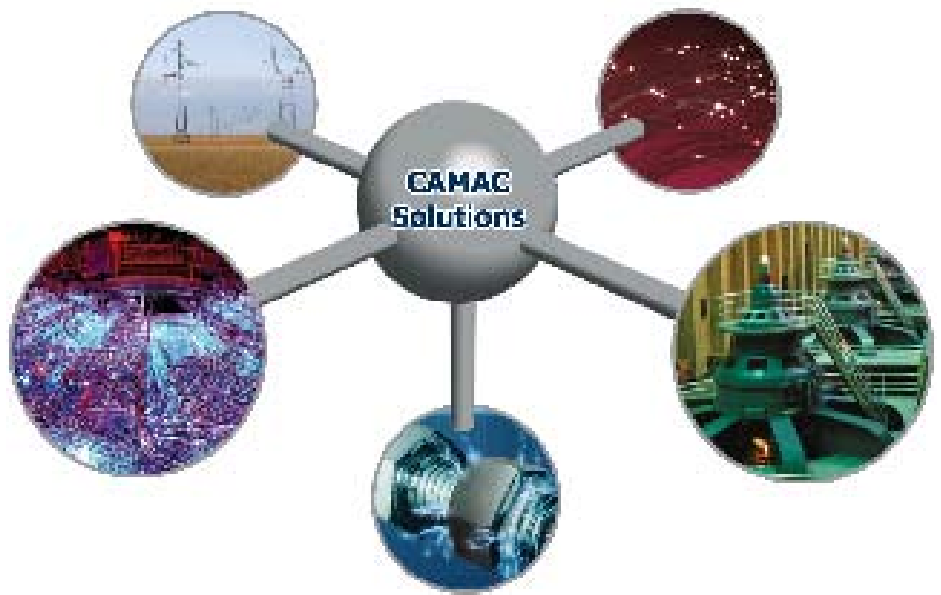
CAMAC, Computer Automated Measurement And Control, is an IEEE-standard (583), modular, high-performance, realtime data acquisition and control system concept.

Since 1969, CAMAC has been used in many thousands of scientific, industrial, aerospace, and defense test systems around the world.

APPLICATIONS

High-speed data acquisition
Event-triggered data acquisition
Mixed NAF block transfers
Distributed control in remote crates

3982 List Sequencing Crate Controller



The Model 3982 is a single-width CAMAC module that functions as an autonomous auxiliary controller within a CAMAC crate.

FEATURES

- Autonomous auxiliary crate controller
- 8192 16-bit NAF memory
- 1024, 2048, or 4096 24-bit CAMAC data memories
- External event, LAM-synchronized or timer-initiated execution of NAF list
- Programmable execution rate
- Q-Repeat mode for delayed transfers
- Front-bus for Read data FIFO readout
- External clock rate input



GENERAL DESCRIPTION

The Model 3982 is a single-width CAMAC module that functions as an autonomous auxiliary controller within a CAMAC crate. Connection to the crate's N (Station Number) and L (Look-at-Me) lines is made through the Auxiliary Controller Bus (ACB) via a main crate controller such as the Model 3920-Series, 3952, 3988, or 3989. Up to 8192 unique commands may be executed from a preloaded NAF list. This list is loaded in Random Access Memory (RAM) from the host computer prior to execution. Commands to be executed may also be optionally drawn from a preprogrammed Programmable Read Only Memory (PROM) mounted in place of the RAM components.

Data associated with commands in the NAF list is stored in one of two 24-bit FIFO memories. Module options determine whether this memory is 1024, 2048, or 4096 words deep. For CAMAC Write commands, data is preloaded into one of the FIFOs before list execution begins. Data from CAMAC Read commands is stored in the other FIFO at S1 time of the Dataway cycle for subsequent readout by the host computer. The CAMAC Read data may also be read out over the Front-bus. The Front-bus is a 50-position front-panel connector that allows the CAMAC Read data FIFO to be read by an external device. RS-485 balanced signaling is used to maintain signal integrity. Optionally, only one FIFO may be used for data storage. In this mode, data received during CAMAC Read commands is used as Write data for subsequent CAMAC Write commands. This option allows the 3982 to read data from one CAMAC module and write that data to another. For CAMAC Control commands no storage space is required in either FIFO.

Once the List Sequencing mode is enabled, list execution can be triggered by CAMAC command, by the receipt of a front-panel TTL level logic signal (200 nanosecond minimum pulse width), or by the assertion of a pre-strapped LAM signal on the CAMAC Dataway. A register on the module allows the user to program the rate at which Dataway cycles occur. This register provides for nominal execution rates ranging from five kilohertz (a Dataway cycle every 200 microseconds) to nearly one megahertz (a Dataway cycle every 1.1 microseconds) in a 1-2-5-10 progression. Optionally, the list execution rate may also be controlled by an external clock input. A bit in the command field provides for the immediate reissuance of a command if that command results in a NO-Q condition. In this mode of operation, no data is strobed into or out of the data FIFOs for the NO-Q cycle. Execution of commands in the list continues in this manner until the "End-of-List" indicator is encountered in the RAM.

List execution begins again, from the beginning of the NAF list, on receiving a new trigger signal or, on the expiration of a Sequence Repeat timer if enabled. This Dataway programmable timer circuit allows the entire NAF sequence to be repeated at a rate ranging from two hertz to 500 hertz. Two straps on the module establish the data storage format for repeated operations. One strap is used to enable/disable the "retransmission" of CAMAC Write data stored in the Write data FIFO to accomplish a repetitive output data pattern. A second strap is used to enable/disable the clearing of the Read data FIFO so that a list of only "currently available data" can be maintained.

Several exceptions cause a cessation of list execution. These conditions include receiving a NO-X response to a Dataway cycle, attempting a CAMAC Write operation while the Write data FIFO is empty, attempting a Read operation while the Read data FIFO is full, and the expiration of the Sequence Repeat timer while the module is still in the list execution process. Exception reporting is available through the module's LAM structure, as is the status of the FIFO Full/Empty and Half-full/Half-empty flags, a List Completion indicator, and an External LAM Source indicator.

POWER REQUIREMENTS

+6 volts — 2800 mA

WEIGHT:

.73 kg. (1 lb. 9 oz.)



ACCESSORIES

Model 5843-Series	Auxiliary Controller Bus Cable Assembly
Model 5857-Axyz/Bxyz	LEMO Cable Assembly
Model 5820-Series	Front-bus Cable Assembly

ORDERING INFORMATION

MODEL	DESCRIPTION
3982-Z1B	List Sequencing Auxiliary Crate Controller, 1K x24 Data Buffers
3982-Z2B	List Sequencing Auxiliary Crate Controller, 2K x24 Data Buffers
3982-Z3B	List Sequencing Auxiliary Crate Controller, 4K x24 Data Buffers
3982-Z4B	List Sequencing Auxiliary Crate Controller, 8K x24 Data Buffers
3982-Z5B	List Sequencing Auxiliary Crate Controller, 16K x24 Data Buffers

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