Part VI: Technical Series on Data Acquisition – Analog to Digital Converter

The Analog-to-Digital Converters (ADC), multiplexer (MUX) and sample-and-hold (S/H) amplifier form major elements of most data acquisition systems. It is important to understand the overall architecture of the ADCs and related components in order to choose an optimum system configuration.

Types of ADCs

The best type of analog-to-digital converter for a given application is determined by the requirements of that application. For example, if a slowly-varying thermocouple input is being measured, then the appropriate ADC might be of the integrating type.

Integrating ADC

This type of converter typically integrates over an integral number of cycles of powerline frequency and provides excellent attenuation of noise at that frequency and its harmonics. These converters may be of the dual-slope or multi-slope type. They provide a high degree of rejection at line frequencies and noise rejection, but have rather poor time resolution and speed.

Successive Approximation ADC

0ne of the most common types of ADC in use today is the successive approximation type. These converters combine high speed with high accuracy, have resolutions from 8 to 24 bits and conversion times from hundreds of microseconds down to submicroseconds. Higher speed ADCs typically have lower resolution. Earlier SAR ADCs were often used with a sample-and-hold amplifier. This element was necessary because the data must be held rather constant during conversion or significant measurement error may occur. The S/H amplifier had to be carefully matched to the ADC, with important parameters such as droop, aperture uncertainty, linearity and gain accuracy. Most modern SAR ADCs are of the charge-redistribution (or switched capacitor) type. This architecture provides high accuracy and linearity at a lower cost and does not require an external S/H amplifier. Many SAR ADCs now offer on-chip input multiplexers as well, making them an ideal choice for multi-channel data acquisition systems.

Flash Converters

Flash converters are usually very high speed with lower resolution. Such converters are generally used to acquire data with scanning rates from 5 Megahertz to multi-Gigahertz. Since the flash converter uses one comparator per bit combination, these converters are often limited to resolutions of 8 bits (256-bit combinations).

Hybrid Converters

Many converters combine several techniques to optimize the resolution, speed and performance. Techniques include multiple-pass converters, error correction, etc.

Sigma-Delta Converters

Sigma-delta (sometimes referred to as delta-sigma) modulation was introduced in 1962, and has gained general market acceptance as a good alternative to successive-approximation ADC's. A sigma-delta converter quantizes an analog signal with very low resolution (1 bit) at a very high sampling rate, typically in the 1 to 12 MHz range. The resultant signal is then passed to a digital lowpass decimation filter. The effect of this filter is to "average" the 1-bit samples, yielding a higher resolution (usually in the 16- to 18-bit range, but as high as 24 bits). This process results in an associated reduction in signal bandwidth and a much lower effective sampling rate. The high sampling rate is described as oversampling. Typically, a sigma-delta converter uses 64 times oversampling.

Sigma-delta technology offers several advantages over a conventional ADC for some applications. Due to the very high oversampling rate and digital filtering, antialias filtering is greatly simplified. A simple one-pole filter at the input usually suffices to attenuate the frequencies in the passband of the digital filter to well below detectable levels. Thus, issues of nonlinear phase can be avoided. Also, Sigma-delta converters exhibit better differential nonlinearity, greater dynamic range and improved signal-to-noise ratios over equivalent ADC subsystems.

Resolution and Accuracy

One of the more confusing tasks when evaluating data sheets is to separate the accuracy of an ADC from its resolution. Just because an ADC exhibits 16 bits of resolution does not guarantee 16 bit accuracy. In fact, an ADC may not even maintain monotonicity (each bit combination measuring a higher value than the next lower combination) over its full operating range, especially over the temperature range. In some applications, resolution is more important than accuracy; it may be more important to be able to resolve small changes in a variable than to know the absolute value of the new signal level. Many 16-bit resolution ADCs exhibit 14 bits of accuracy, and this is sufficient for a large number of applications.

In some applications absolute accuracy is paramount; therefore overall accuracy becomes more important than resolution. In these cases, it is important to look at the integral nonlinearity specification. This represents an error which cannot, in general, be eliminated with calibration.

Understanding the overall system requirements will aid in the selection of the appropriate ADC without overspecifying its characteristics. Higher cost is generally associated with ADCs that have more stringent characteristics. If dynamic accuracy is important, then it may be better to choose a faster, lower-resolution ADC than one with high resolution but longer conversion time.

Multiplexing Analog Signals

The analog to digital converter is often a relatively expensive component. In multichannel applications it is frequently more economical to multiplex many analog signals into a single ADC. At slower scan rates this can be very economical because the ADC, sample-and-hold amplifier and front-end gain stages can be shared by a large number of channels. Modern ADC modules of this type typically include a multiplexer, a programmable-gain amplifier and an ADC. The gain for each analog channel is stored in on-board RAM memory, and the gain is set individually for each input channel to the MUX. At higher scan rates, the settling time following a gain change and slew-rate limits of the amplifier section reduce the effectiveness of this architecture.

At intermediate scan rates, particularly in high gain situations, a separate amplifier must be provided for each channel. Also, in applications which require low-pass filters, these elements must be on a per channel basis and cannot be shared. At high sampling rates, settling times preclude the use of multiplexers. In such cases, it is more appropriate to use an ADC per channel. As was discussed earlier, sigma-delta converters may represent a better choice than multiplexing for some applications, even at lower scan rates.

Sequential Scan vs. Simultaneous Sample-and-Hold

In many applications, it is sufficient to sequentially scan and convert each channel with a multiplexed ADC. Using this approach, successive channels are sampled at consecutive time increments during each scan. The ADC may be self-scanning, or the scan may be initiated based on a system trigger. Self-scanning ADCs are generally appropriate for low sampling rate applications where "the most recent value of the signal" is acceptable—the exact time of the sample is unknown to within the scan interval, typically several microseconds.

In more demanding data acquisition applications, it is important to sample data at evenly spaced intervals. Also, some time-skew between successive channels may be acceptable, as long as the interval between samples on any given channel is stable. In these applications, the ADC scan is triggered by a hardware clock. Typical aperture uncertainly (variation in sampling interval) for a given channel is approximately half the ADC clocking rate.

Simultaneous Sampling

In some very demanding applications, it is essential that the signals from *all* channels be sampled simultaneously and that the time-jitter in sampling of each channel be tightly controlled. In these cases, it is necessary to use a sample-and-hold (S/H) amplifier associated with each channel with all the (S/H) amplifiers clocked simultaneously. This approach typically reduces the aperture uncertainty or jitter into the sub-nanosecond range.